Resistive Products

Technical Note

Pulse Load Capability of Precision Chip Resistors

By Joseph Szwarc, 2008

ABSTRACT

Three test procedures were used to assess the Pulse Load Capability (PLC) - the stability of precision foil and Thin Film chip resistors under pulses of increasing voltages for duration below 0.1 s, in three time ranges: milliseconds, microseconds and nanoseconds:

- Test # 1 - Rectangular pulses of durations between 100 ms and 0.1 ms
- Test # 2 - Exponential pulses (by capacitor discharge) of energy equivalent to rectangular pulses of duration 150 µs, 25 µs, 5 µs and 1 µs and voltages increased up to 5500 V or until one of the chips in a group of 20 showed a drift of 0.01 %, 0.1 %, 1 % and 10 %
- Test # 3 - For pulse durations in the nanoseconds range Electrostatic Discharge (ESD) testing was performed per recommendations of the International (IEC) generic and European (EN) detail standards. Voltage levels from 2 kV to 24 kV were applied and at each level the resistance drift was recorded

Test results indicate that for pulse durations down to 1 ms the foil and the Thin Film chips perform similarly, but for shorter pulses the foil chips show an advantage over Thin Film chips. This advantage increases with shortening of pulse duration and approaching an adiabatic process. Foil's advantage stems from the bulk metal properties of the resistive material resulting in high stability and from its high thermal capacity as it is about hundred times thicker than the Thin Film layer.

In longer pulses the difference is small as the substrate has the time to absorb the heat. The Pulse Load Capability test results are compared with the recommendations of international and other standards concerning pulse load rating of chip resistors. Two articles published in the past (references 1 and 2) about pulse loading of resistors are reviewed. Failure analysis was performed to determine the failure modes under high power pulses and recommendations are suggested for design improvements to increase the pulse load capability.

LIST OF ABBREVIATIONS

DUT	Device Under Test
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
MLCP	Maximum Load for Continuous Pulses
MLSP	Maximum Load for Single Pulses
MPPV	Maximum Permissible Pulse Voltage
OEM	Original Equipment Manufacturer
O/L	Overload
PEO/L	Periodic Electric Overload
PLC	Pulse Load Capability
Pn	Nominal Power Rating
SPHVO	Single Pulse High Voltage Overload Test
TCR	Temperature Coefficient of Resistance

INTRODUCTION

The datasheets of precision resistors usually specify the initial tolerance of the ohmic value, the Temperature Coefficient of Resistance (TCR), the Nominal Power (Pn) rating and the maximum resistance drift after loading at Pn and at a high ambient temperature during a stated time. Resistor's design and manufacturing methods tend to achieve the best above mentioned specifications at lowest cost without optimizing for Pulse Load Capability.

For a circuit designer these specifications are adequate in applications of continuous resistor's load, but not in case of high intermittent load - for instance consisting of pulses of a given power, duration and periodicity - or in case an immunity to external disturbances, like Electrostatic Discharge (ESD) or Electromagnetic Compatibility (EMC) is required for entry into a given country's market.

These requirements address usually electronic devices, not the components like resistors used in these devices - but manufacturers of the devices often include some ESD and EMC specifications in their resistor's qualification requirements.

TECHNICAL NOTE

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EMC testing of electronic devices is addressed by many different categories of standards:

- International: ISO, CISPR/IEC 61000 (IEC 60601-1-2 for medical equipment)
- European Union directives (EN, IEC)
- USA: MIL-STD-883, ANSI, FDA (for medical devices), FCC (for telecommunication), SAE (automotive)
- Specific to OEM

Test equipment manufacturers build pulse generators to fit different standards. In the USA, the resistor standards MIL-PRF-55432 and EIA-575 do not refer to short pulses - only to a 5 s Short Time Overload test at 6.25 times the Pn.

European specifications, based on the IEC 61000 which recommend test procedures and stress levels for PLC, ESD and EMC testing of fixed resistors for use in electronic equipment, are generic specification EN 60115-1 and, for precision chip resistors (of stability classes 0.1 % to 1 %), the detail specification EN 140401-801 A1.

PRODUCTION TECHNOLOGIES AND STANDARD SIZES OF CHIP RESISTORS

The table below shows typical specifications for two main technologies used in production of precision surface mounted chip resistors: Bulk Metal Foil and Thin Film.

TABLE 1 - COMPARISON OF ELECTRICAL SPECIFICATIONS OF FOIL AND THIN FILM CHIPS

PRODUCTION TECHNOLOGY	BEST TCR, MIL. RANGE, ppm/°C	RANGE OF OHMIC VALUES, ALL CHIP SIZES
Bulk Metal Foil	0.2	5 Ω to 150 kΩ
Thin Film	10	30 Ω to 3 MΩ

Foil chips are produced by cementing to a ceramic substrate a Nickel-Chromium alloy foil, rolled to a thickness between 2 microns and 10 microns.

Thin Film chip production involves deposition (by evaporation, sputtering or similar methods) on a ceramic substrate of a film, mainly Nickel-Chromium or Tantalum Nitride.

A typical thickness of the Thin Film layer is about 1/100 of foil's thickness. The EN 140401-801 A1 covers 5 standard styles of chips - sizes from 1 mm by 0.5 mm (style RR 1005M, English style RR0402) to 5 mm by 2.5 mm (style RR5025M/RR2010). The next to largest size, RR3216M (RR1206) was chosen for testing and test results are compared with recommendations of standards and specifications.

PULSE LOAD CAPABILITY AND TESTING PER INTERNATIONAL STANDARDS

The international generic specification of fixed resistors, IEC 60115-1 and its modification, the European EN 60115-1 define several test and measurement procedures.

The detail chip resistors' specification EN 140401-801+A1 and the draft prEN 140401-801:200X refer to EN 60115-1 and provide specifications for PLC testing of precision chip resistors. The EN 140401-801+A1 contains three logarithmic scale PLC graphs in Time - Power coordinates covering a range of pulse durations from 10 µs to 100 ms, with 4 curves for 5 sizes of chips (one curve for two largest sizes, RR3216M and RR5025M).

- Maximum Load for Continuous Pulses (MLCP), rectangular or equivalent, for which the average load does not exceed the nominal load
- Maximum Load for Single Pulses (MLSP)
- Maximum Permissible Pulse Voltage (MPPV)

The curves of the two first graphs consist of horizontal segments for pulse durations between 10 µs and 200 µs, falling straight lines between 0.6 ms and 100 ms (0.1 s) and transition curves joining the horizontal and falling straight lines.

The horizontal segment indicates a constant load - from 2.2 W (for the smallest chip size) to 18 W (for the largest) for MLCP and 3.8 W to 30 W respectively for MLSP.

The falling lines start from load values about 20 % below the mentioned single pulses' constant load values and descend to values of 0.2 W for the smallest chip size and to 1.7 W for the largest size for MLCP, and to 0.38 W and 3 W respectively for MLSP. These load values at 0.1 s are 6 to 12 times larger than the respective rated continuous dissipation values at 70 °C.

Fig. 1 shows, for the chip size RR3216M (RR1206 English size) the two segments of the MLSP chart - $MLSP_c$ for the constant load segment and $MLSP_f$ for the falling one. The slope of the $MLSP_f$ line represents approximately a $t^{-0.4}$ time dependence of pulse power P:

$\log(P_2/P_1) = -0.4 \times \log(t_2/t_1)$ or: $P_2/P_1 = (t_2/t_1)^{-0.4}$.

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The third graph puts, for the two largest chip sizes, the maximum permissible pulse voltage at 700 V for pulse durations from 10 µs to 300 µs, declining to 240 V for 0.1 s duration. For the smallest chip size the voltages are about 180 V and 60 V respectively.

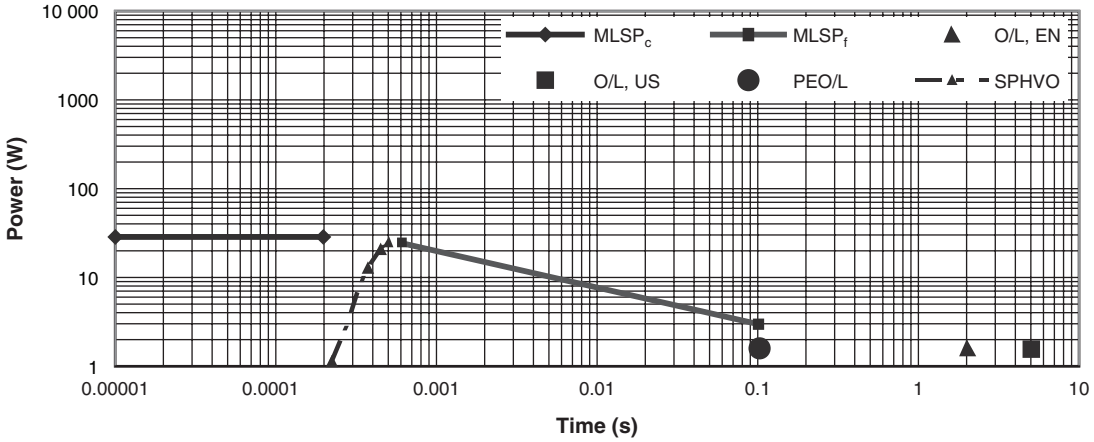

Fig. 1 - Safe Pulse Power per EN Specification, Chip Size RR3216M (RR1206)

Additional pulses are specified in Qualification Approval and Quality Conformance Inspection tests (referenced to EN 60115-1) of Annex A of the EN 140401-801+A1 specification:

- Overload (O/L): Load of 6.25 times the rated dissipation (for ohmic values up to the critical value), duration from 0.5 s for the smallest size to 2 s for RR3216M (see O/L point in fig. 1). Maximum allowed resistance change depends on Stability Class (1, 0.5, 0.25 and 0.1) and for class 0.1 is ± 0.05 % R + 0.01 Ω. In the USA the specification MIL-PRF-55432 of chip resistors requires a duration of 5 s for a similar test and no other pulse tests are specified (see point O/L, US on fig. 1)
- Periodic Electric Overload (PEO/L): Pulses of 0.1 s: 1000 cycles at a load of 15 times the rated dissipation at 70 °C, 0.1 s on and 2.5 s off. This load, compared to the continuous pulses graph at 0.1 s has a value close to it for two smallest sizes and down to half for larger chip sizes. Such continuous pulses result in an average load: P_{AV} = 0.1/(0.1 + 2.5) = 1/26 of pulse power and 6.25/26 = 0.24 of nominal the nominal power rating (see PEO/L point in fig. 1). Maximum allowed resistance change is ± (1 % R + 0.05 Ω).
- Single pulse high voltage overload test (SPHVO): Pulse of wave-form 10 µs/700 µs per EN60115-1 specification. The voltage applied is 10 times the rated or twice the maximum voltage and it charges a 20 µF capacitor. The discharge circuit contains, beside the tested resistor, two series resistors of 40 Ω total and a shunting resistor of 50 Ω. As a result, the pulse duration increases slightly with increase of chip's ohmic value. The percentage of capacitor's discharge energy dissipated by the tested chip resistor decreases, but not its absolute value because the level of charge voltage is based on chip's rated voltage. Fig. 1 shows four points for 4 randomly chosen ohmic values (10 Ω, 100 Ω, 400 Ω and 16 000 Ω), the duration and the power of an equivalent rectangular pulse that the tested resistor will have to dissipate. The duration changes from 222 µs for 10 Ω to 500 µs for 160 000 Ω. The latest value is the critical value for this chip size - the chip will dissipate the nominal rated power of 0.25 W when the maximum voltage of 200 V is applied to it, while in this test the capacitor is charged at 2 kV (10 times the rated voltage), a voltage of 1999.5 V will build up across the tested resistor, but due to the 50 Ω shunt a very small current will flow in it. Low value resistors will be stressed with low voltages - for instance for a 100 Ω resistor the test voltage will be 50 V (36 V across the chip). Maximum allowed resistance change is ± (0.5 % + 0.05 Ω)

Among the PLC tests recommended by the generic resistor's specification but not in the detail chip resistor's specification is the 1.2 µs/50 µs "lighting pulse", similar to the SPHVO and sometimes requested by the OEM. In this case a 2 µF capacitor is charged and the discharge circuit contains, beside the tested resistor, two resistors of 37.5 Ω total in series with it and a shunting resistor of 33 Ω. Like in the SPHVO test, the pulse duration and percentage of capacitor's discharge energy dissipated by the tested chip resistor both depend on its ohmic value, but not so the charge voltage, which in this case is a multiple of chip's maximum voltage.

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TEST # 1 - FOR PULSES OF DURATION BETWEEN 0.1 ms AND 100 ms

Rectangular pulses of durations 0.1 ms, 1 ms, 10 ms and 100 ms were applied to 1000 Ω Foil and Thin Film resistors - groups of 5 chips, size RR3216M/RR1206. Power levels were increased after measurement by 10 % each time until one chip in a group of five showed a drift of more than 0.1 % + 0.05 Ω.

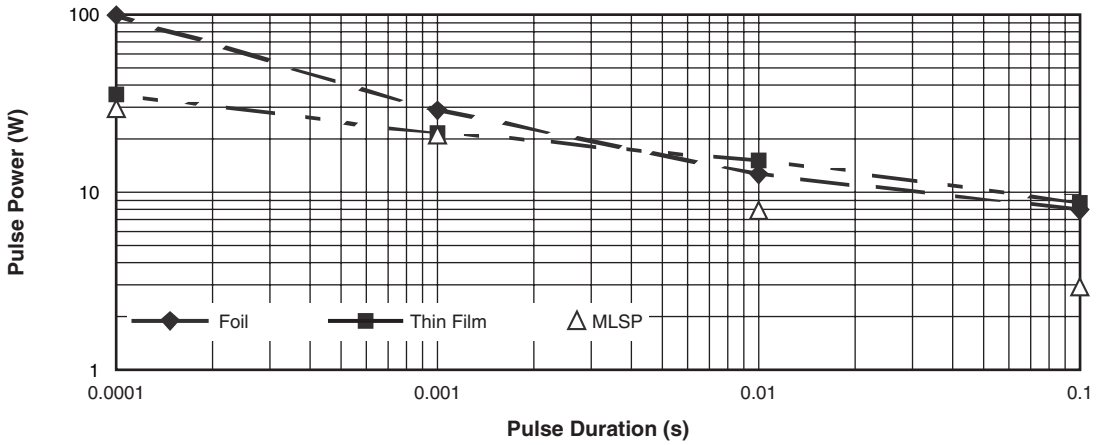

Fig. 2 - Pulse Power of Foil and Thin Film Chips, Size 1206, 1 kΩ

Each time 100 pulses were applied in time intervals long enough to reduce the average power to less than 10 % of rated power. In fig. 2 the results are represented by two broken lines and the triangles represent the corresponding values from the MLSP graph.

The graph shows a similar performance of Foil and Thin Film from 0.1 s down to about 0.003 s and a superior performance of Foil for shorter pulses where the data of Thin Film is close to MLSP's. At 0.0001 s the MLSP specifies 30 W, Thin Film supported 36 W and Foil 100 W.

The EN specification does not affix any limit of resistance change to the MLSP chart's values, but the limit for SPHVO, which (except for low values) is equivalent to pulse duration of 0.0005 s, has a drift limit of ± (0.5 % R + 0.05 Ω).

TEST # 2 - FOR PULSES OF DURATION BETWEEN 1 µs AND 150 µs

For this test an in-house built pulse generator was used. Chips of different resistance values were matched with different capacitances in the pulse generator in order to achieve exponential pulses equivalent to rectangular pulses of duration t.

Per specification EN140401-801, duration t of an equivalent rectangular pulse is t = 0.5 RC:

0.5 x 33 Ω x 0.06 µF = 1 µs
0.5 x 1000 Ω x 0.01 µF = 5 µs
0.5 x 5000 Ω x 0.01 µF = 25 µs
0.5 x 30 000 Ω x 0.01 µF = 150 µs

Voltage levels were increased after measurement by 10 % each time until one chip of a group of 20 showed a drift of more than 0.01 %, and increases were continued for drifts of 0.1 %, 1 % and 10 %. Highest voltage before a given drift occurred was recorded as a safe voltage and the corresponding safe power, $P_S = U_S^2/R$, was computed.

In case the maximum pulse-generator's voltage of 5500 V did not cause a given drift, it was recorded as the safe voltage.

In fig. 3A and 3B the results are represented in two charts - A for drifts less than 0.01 % and less than 0.1 % and B for drifts less than 1 % and less than 10 %. Broken lines represent Thin Film and continuous lines represent Foil chips.

Safe power for drift of 1 % and 10 %, 150 µs pulse for foil chips is not shown because the maximum available voltage (5500 V) of the pulse generator did not suffice to cause a relevant drift.

A horizontal line joining two round points in fig. 3B represents, for reference, a segment of the MLSPc line (see fig. 1).

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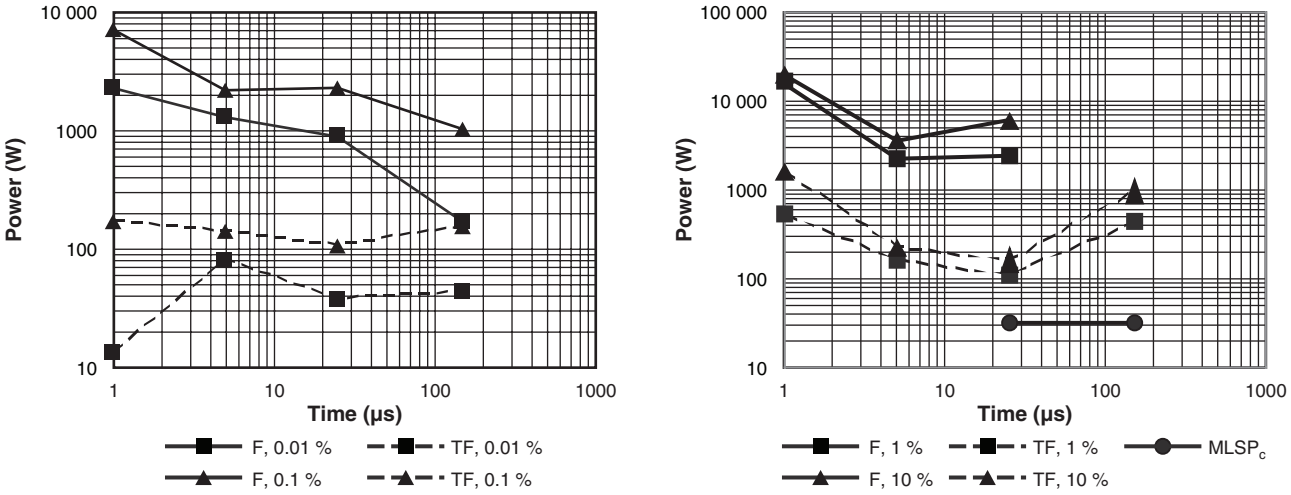

A. Drift less than: 0.01 % (square points) and 0.1 % (triangular points)

B. Drift less than: 1 % (square points) and 10 % (triangular points)

Fig. 3 - Safe Pulse Power, durations 1 µs to 150 µs, Foil (continuous line) and Thin Film (broken line) chips, size RR3216M/RR1206

The graph shows a superior performance of Foil over Thin Film chips, especially for applications requiring high stability - low drift. The Thin Film performed poorly at the shortest pulse and drift level of 0.01 % (see the “TF, 0.01 %” line), but this may be due to the low value of the tested chips - see “conclusions” below.

Apart from this point all samples performed far above the MLSP specifications. The large scatter may be attributed to the fact that a different ohmic value was used for each pulse duration.

TEST # 3 - FOR PULSES OF DURATION IN THE NANOSECONDS RANGE

These tests were performed per specifications EN140401-801-200X and EN60115-1. A test simulator conforming to the above mentioned specifications produces an adjustable voltage ESD pulse by discharging a 150 pF capacitor to the Device Under Test (DUT) with a discharge resistor of 330 Ω connected in series. (These parameters differ from the ANSI/ESD 20-1999 standard which specifies a 100 pF capacitor and a 1500 Ω discharge resistor)

The waveform of the ESD simulator is verified by discharging the capacitor while a 2 Ω calibration resistor replaces the DUT. The resulting pulse has therefore a time constant of:

RC = (330 + 2) x 150 x 10^{-12} Ω x (s/Ω) = 49.8 x 10^{-9} s (about 50 ns compared to 150 ns per ANSI standard).

The ESD exponential waveform which was calibrated with a discharge resistance of 330 Ω + 2 Ω will have a time constant which is double when the DUT is a resistor of 332 Ω and much longer with a high ohmic value DUT.

The prescribed test voltages are from 500 V for the smallest chip size to 3000 for the largest. The limit of allowed change of resistance is set for all chip stability levels at 0.5 %.

The test voltage assigned for the RR3216M/RR1206 size is 2 kV, and we used this voltage as a starting point of our test, submitting the chips to gradually increased voltages up to 24 kV or up to a failure of two (or more) chips in a lot, and recorded all resistance values.

At each voltage level three positive and three negative pulses were applied.

In order to compare the ESD susceptibility of chips coming from different technologies, samples of 3 types were tested:

A. Foil

B. TF1 Thin Film - Nickel-Chrome

C. TF2 Thin Film - Tantalum Nitride

Each lot contained 20 chips, bringing the total (for two values and three types) to 120 DUT. Tables 2, 3 and 4 show, for three levels of ESD discharge voltages, and for types which survived a lower voltage level, the number of resistors which shifted by more than 0.5 % and the distribution by % of deviation of DUT which shifted by less than 0.5 %.

The Foil chips under a stress of 24 kV drifted less than Thin Film chips under a stress of 2 kV or 3 kV. As power is proportional to the square of the voltage, the ratio of stress, in Watts, is $(24/2)^2 = 144$ or $(24/3)^2 = 64$.

For instance, after ESD up to 24 kV (see table 4), all the 20 foil chips of 30 Ω shifted less then 0.2 %:

One shifted less than 0.01 %, 3 - between 0.01 % and 0.02 %, 14 - between 0.02 % and 0.05 %, and 1 each - between 0.05 % and 0.1 % and between 0.1 % and 0.2 %.

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TABLE 2 - 2 kV ESD DISCHARGE - COMPARISON OF DEVIATIONS, FOIL VS. THIN FILM							
	DISTRIBUTION OF 20 CHIPS BY % OF DEVIATION AFTER ESD DISCHARGE						
TYPE AND VALUE	> 0.5 %	0.2 % to 0.5 %	0.1 % to 0.2 %	0.05 % to 0.1 %	0.02 % to 0.05 %	0.01 % to 0.02 %	< 0.01 %
Foil, 30 Ω	0	0	0	0	1	6	13
TF1, 30 Ω	12	8	0	0	0	0	0
TF2. 30 Ω	0	1	1	2	8	4	4
Foil, 1000 Ω	0	0	0	0	0	0	20
TF1, 1000 Ω	20	0	0	0	0	0	0
TF2, 1000 Ω	20	0	0	0	0	0	0

TABLE 3 - 3 kV ESD DISCHARGE - COMPARISON OF DEVIATIONS, FOIL VS. THIN FILM							
	DISTRIBUTION OF 20 CHIPS BY % OF DEVIATION AFTER ESD DISCHARGE						
TYPE AND VALUE	> 0.5 %	0.2 % to 0.5 %	0.1 % to 0.2 %	0.05 % to 0.1 %	0.02 % to 0.05 %	0.01 % to 0.02 %	< 0.01 %
Foil, 30 Ω	0	0	0	0	1	8	11
TF2. 30 Ω	4	10	3	2	1	-	-
Foil, 1000 Ω	0	0	0	0	0	0	20

TABLE 4 - 24 kV ESD DISCHARGE - COMPARISON OF DEVIATIONS, FOIL VS. THIN FILM							
	DISTRIBUTION OF 20 CHIPS BY % OF DEVIATION AFTER ESD DISCHARGE						
TYPE AND VALUE	> 0.5 %	0.2 % to 0.5 %	0.1 % to 0.2 %	0.05 % to 0.1 %	0.02 % to 0.05 %	0.01 % to 0.02 %	< 0.01 %
Foil, 30 Ω	0	0	1	1	14	3	1
Foil, 1000 Ω	0	0	0	0	0	0	20

Three Thin Film lots failed the 0.5 % limit at 2 kV, the fourth at 3 kV.

The 30 Ω Foil lot shifted less than 0.05 % at 2 kV and 3 kV, and less than 0.2 % at 24 kV.

The 1 kΩ Foil lot shifted less then 0.01 % up to 24 kV.

OBSERVATIONS OF FAILURE ANALYSIS

The most common observed failure mode was a dislocation or evaporation of resistive material in a location suggesting a “hot spot” - heat generated in a spot of high energy density. It was especially evident in low value Thin Film chips with laser cut resistive patterns: a current crowding occurs at the top of a laser cut (kerf) where the current changes its direction.

During a very short and high voltage pulse a spark occurs sometimes across the kerf - especially in low-ohm patterns containing few lines and therefore a high potential difference between adjacent lines or over the kerf cut by the laser in a loop which shunts a part of the pattern (a high electrical field is created in the kerf).

SHORT REVIEW OF FORMER PUBLICATIONS (see bibliography below)

The paper of ref. 1, dated 1975, describes studies of failures of resistors after application of increasing pulse power of duration between 1 µs to 10 ms. A 5 % change of resistance was considered a failure and the following families of resistors are discussed: carbon composition, wire-wound and Thin Film (cylindrical).The major changes in resistor manufacturing technologies for the electronic market were the trend of miniaturization and surface mounted technology. However many conclusions of the investigation are relevant also today for the precision chip resistors. For instance the problem of power crowding in spiraled film resistors and the $t^{-1/2}$ time dependence of pulse power for pulses over 20 µs long.

The paper of ref. 2, dated 1995, discusses the European Standards and law concerning Electromagnetic Compatibility (EMC) of electronic devices, their relevance for components, and particularly to resistors. Experimental findings are presented of Pulse Load Capability (PLC) in the nano-second range by application of several ESD pulses

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and measuring the resistance drift after each pulse.

In the microseconds range the pulse 1.2 µs/50 µs was applied.

Types of resistors tested and compared were 0603 size chips - metal film, a proprietary cermet film and thick film.

The book of ref. 3 proposes to calculate resistor's temperature rise for single pulses of duration below 0.1 s based on an adiabatic process and the weight of the wire. A calculation for a wire-wound resistor is presented. This suggests a t^{-1} time dependence of pulse power (constant energy), as opposed to t^{-04} relationship for chip resistors.

CONCLUSIONS AND RECOMMENDATIONS

The data sheets of resistors available on the market provide a limited information (or no information at all) about pulse load capability. It is not practical to cover all the parameters of required specification - pulse shape, duration, power and repetition rate. Therefore the first step recommended to a circuit designer is to check if there is a standard specified pulse close enough to the needed one and to request capability information per his specification and this standard.

As the resistor's design is not usually optimized for short pulses, it is sometimes possible to improve short pulse capability by special design for a small increase in manufacturing costs: for instance "hot spots" in the resistive pattern are admissible at continuous rating but create high temperature gradients in short pulses. Improved design is uneconomical for general applications, but may provide a solution for a short pulse application.

For pulses of durations below 1 ms the mass of the resistive layer becomes increasingly important and the choice of foil resistors, with their relatively thick resistive layer and a pattern avoiding hot spots can lead to a reduction in chip's size.

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